Extraction and LVS

ECE 09414 - 2 VLSI

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I. Abstract

Through the use of extraction and LVS the schematic for a circuit can be generated through Cadence. This allows for testing to be done without the need to create the schematic by hand. This allows for a streamlined circuit development with similar outcomes to manually generated circuit schematics.

II. Introduction

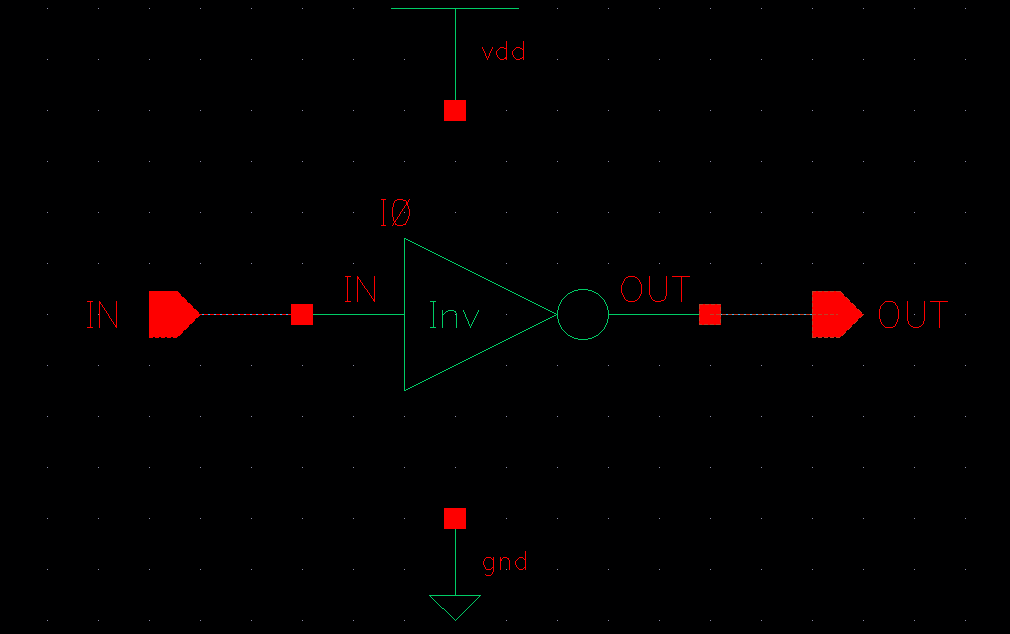
With the use of the extraction and LVS tools the inverter layout that was previously created was used to validate the schematic this inverter was based off of. This layout was improved upon and then extracted once all of the layout guidelines were met. This extracted layout was then used by the LVS (layout vs. schematic) tool to validate a schematic file for the desired inverter circuit. This allows for designers to validate these schematics from the layouts when developing circuits to test them.

III. Procedure

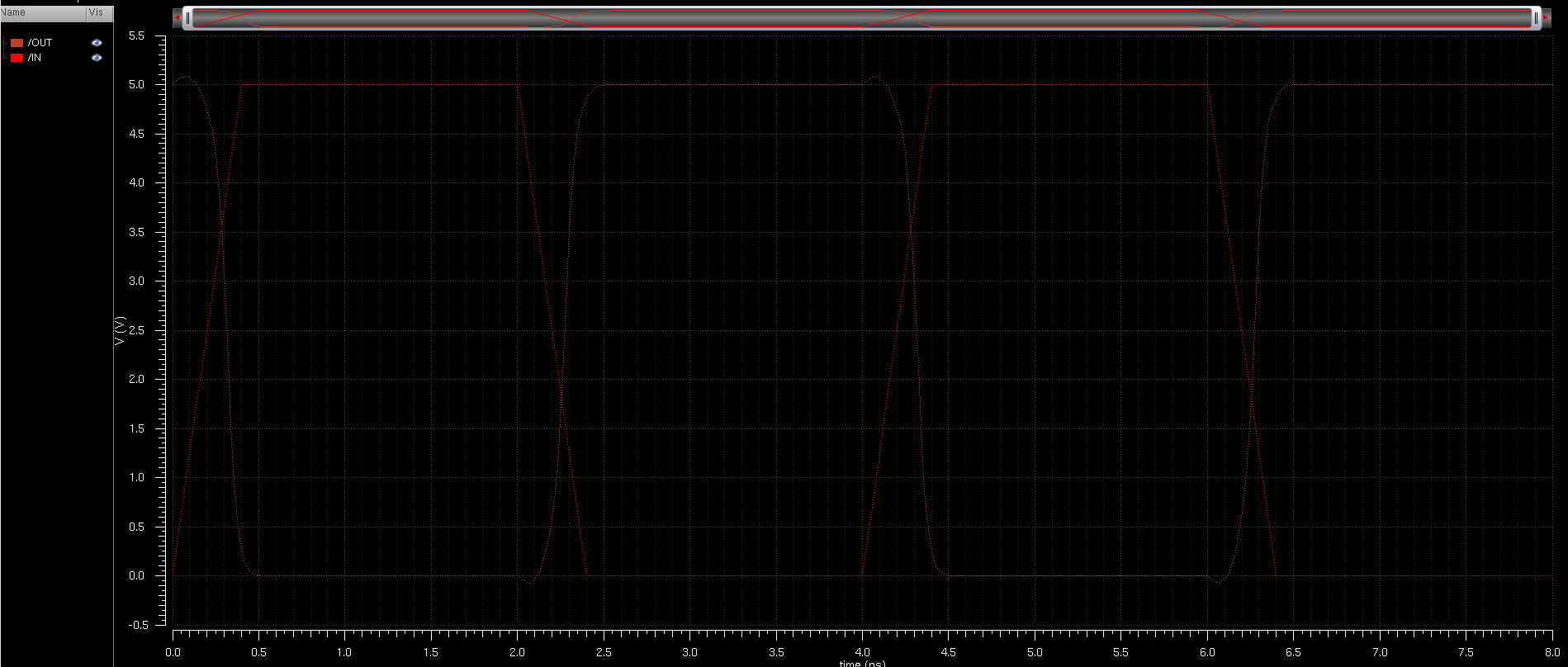
The previous schematic that was created to show the layout of the inverter was improved upon by reducing the amount of polysilicon used. This was done by placing the polysilicon connector closer to the bridge and using metal to connect the connector outside of the circuit. Additional connectors were placed to denote the pins of the layout as well. This allows for these connectors to be made when the schematic is generated as to alleviate the extra work of identifying pins. After the changes were made to the layout the extraction was ran to extract parasitic caps from the layout. From this point the layout was compared against the existing schematic to check for accuracy. The pins were verified to exist and be named correctly to correspond each pin on the layout with a pin on the schematic.

With a validated schematic file for the inverter the inverter was then tested to ensure it works as it was intended to. A pulse signal was put through the inverter while both the input and output were monitored. This allowed for the graph to be created which shows the state change of the inverter output as the pulse signal input changed state. This verifies that the layout will work as intended when made into a physical circuit so long as no issues arise during the fabrication process.

IV. Results



**Figure 1:** The generated inverter being tested by putting a pulse signal through it while monitoring both the input and the output to see the rise and fall of the output. This ensures that the layout works as intended.



**Figure 2:** The generated inverter’s input and output signals as they were tested with the pulse signal input. This shows the inverter working just as it was intended with no real difference between its operation and the manually generated inverter.

V. Conclusions

With the extract and LVS tools in place the circuits created can be easily checked to ensure they function as intended. This allows for layouts that are created to be checked against the schematic they are produced from in order to make sure that the circuit that is to be produced is guaranteed to work when the chip is fabricated. With this feature designers are able to be sure their designs will work before they are passed onto the fabrication process that would cost their company large sums of money if there was even a slight issue in the chip.